IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: **GAILHARD ET AL.**

Serial No. **Not Yet Assigned**

Filing Date: **Herewith**

For: **PRECISE DIGITAL GENERATOR PRODUCING CLOCK SIGNALS**

I HEREBY CERTIFY THIS PAPER OR FEE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED BELOW AND IS ADDRESSED TO: BOX PATENT APPLICATIONS, ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.

EXPRESS MAIL NO: EL747059541US

DATE OF DEPOSIT: October 30, 2001

NAME: Brian M. Sampson

SIGNATURE: [signature]

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

Submitted herewith is a request for proposed drawing modifications as indicated in red ink to label the blocks in FIGS. 1-5. FIGS. 1, 3 and 5 are being further amended to better illustrate the plurality of lines between the applicable blocks.

In the Claims:

Please cancel Claims 1 to 17.

Please add new Claims 18 to 53.

18. A signal generator comprising:
an oscillator for providing an output signal from an

N-bit control number, with N being an integer greater than 1, said oscillator comprising

a first group of cells, each cell comprising at least one inverter,

a first selection circuit connected to said first group of cells for selecting a number of cells as a function of predetermined most significant bits of the control number,

a second group of cells, each cell comprising at least one inverter, and

a second selection circuit connected to said second group of cells for selecting one of the cells within said second group of cells as a function of predetermined least significant bits of the control number,

selected cells of said first and second groups being connected in series to form a chain of inverters.

19. A signal generator according to Claim 18, wherein each cell within said second group of cells is assigned a place value j ranging from 1 to NL.

20. A signal generator according to Claim 19, wherein said second selection circuit comprises NL switches controlled by signals representing the least significant bits of the control number, each switch being series connected with a cell having a same place value j between an input and an output of the second group of cells.

21. A signal generator according to Claim 18,

wherein two different cells within said second group of cells have different propagation times for a first logic value and a second logic value.

22. A signal generator according to Claim 19, wherein a difference between a propagation time of a first logic value and a second logic value in a cell within said second group of cells having a place value j and that of a cell within said second group of cells having a place value j-1 is less than a desired uncertainty for a period of the output signal.

23. A signal generator according to Claim 19, wherein when the control number increases by 1, a cell within said second group of cells with a place value j is selected, this selected cell being at least one of a cell having a place value immediately higher than that of a previously selected cell within said second group of cells, and a cell with a lower place value, with an additional cell within said first group of cells also being selected.

24. A signal generator according to Claim 18, further comprising a comparator for comparing a period of the output signal with a desired period for providing the N-bit control number in the form of N logic signals, with the control number increasing if the period of the output signal is less than the desired period, decreasing if the period of the output signal is larger than the desired period, and remaining constant otherwise.

25. A signal generator according to Claim 19,

further comprising a first decoder for decoding the least significant bits NL0 of the control number and for providing a first set NL = 2^{NL0} of control signals (SDL(1) to SDL(NL)) to said second selection circuit, this first set of control signals having the following properties: SDL(j) = 1 if j = NRL+1 for any value of j ranging from 1 to NL, with NRL corresponding to a decimal value of the NL0 least significant bits of the control number.

26. A signal generator according to Claim 25, further comprising a second decoder for decoding the most significant bits NH0 of the control number and for providing said first selection circuit a second set NH = 2^{NH0} of control signals (SDH(1) to SDH(NH)), this second set of control signals having the following properties: SDH(i) = 1 if i = NRH+1 for any value of i ranging from 1 to NH, with NRH corresponding to a decimal value of the NH0 most significant bits of the control number.

27. A signal generator according to Claim 18, further comprising a control circuit for verifying the following inequality and producing a first control signal if the inequality is not verified:

$$0 \leq (TC0+TC1) + (TD0(1)+TD1(1)) - (TD0(NL)+TD1(NL))$$

wherein:

TC0+TC1 is a propagation time of a first logic value and a second logic value in a cell within said first group of cells,

TD0(1)+TD1(1) is a propagation time of a first

logic value and a second logic value in a least significant cell within said second group of cells, and

TD0(NL)+TD1(NL) is a propagation time of a first logic value and a second logic value in a most significant cell within said second group of cells.

28. A signal generator according to Claim 27, wherein said control circuit comprises:

a reference oscillator for providing a signal with a reference period proportional to (TC0+TC1) + (TD0(1)+TD1(1));

a first measurement oscillator for providing a signal having a measured period proportional to (TD0(NL)+TD1(NL)); and

a first comparison circuit for comparing the measured period with a reference period and for providing the first control signal if the measured period is smaller than the reference period.

29. A signal generator according to Claim 27, further comprising a comparator for comparing a period of the output signal with a desired period for providing the N-bit control number in the form of N logic signals, and said comparator increases the N-bit control number by one unit when the control signal is received.

30. A signal generator according to Claim 28, wherein said control circuit further comprises:

a second measurement oscillator for providing a signal having a second measured period proportional to (TD0(NL-1)+TD1(NL-1)); and

a second comparison circuit for comparing the second

period with the reference period, and for providing a second control signal if the measured period is less than the reference period.

31. A signal generator according to Claim 30, wherein said control circuit is activated when said oscillator starts to operate, and at least one of the first and second control signals is memorized.

32. A signal generator according to Claim 31, wherein the first control signal is taken into account when the cell with the place value NL-1 within said second group of cells is selected.

33. A signal generator according to Claim 31, wherein the second control signal is taken into account when the cell with the place value NL-2 within said second group of cells is selected.

34. A signal generator according to Claim 31, wherein said control circuit is activated when the cell with the place value NL-1 within the second group of cells is selected.

35. A signal generator according to Claim 31, wherein said control circuit is activated when the cell with the place value NL-2 within said second group of cells is selected.

36. A signal generator comprising:
a comparator for comparing a period of an output

signal with a desired period for providing an N-bit control number;

a first decoder for decoding predetermined least significant bits of the N-bit control number and for providing a first set of control signals;

a second decoder for decoding predetermined most significant bits of the N-bit control number and for providing a second set of control signals; and

an oscillator for providing the output signal from the N-bit control number, with N being an integer greater than 1, said oscillator comprising

a first group of cells, each cell comprising at least one inverter,

a first selection circuit connected to said first group of cells for selecting a number of cells based upon the second set of control signals,

a second group of cells, each cell comprising at least one inverter, and

a second selection circuit connected to said second group of cells for selecting one of the cells based upon the first set of control signals, each cell within said second group of cells being assigned a place value j ranging from 1 to NL,

selected cells of said first and second groups being connected in series to form a chain of inverters.

37. A signal generator according to Claim 36, wherein said second selection circuit comprises NL switches controlled by the first set of control signals.

38. A signal generator according to Claim 36, wherein two different cells within said second group of cells have different propagation times for a first logic value and a second logic value.

39. A signal generator according to Claim 36, wherein the control number increases if the period of the output signal is less than the desired period, decreases if the period of the output signal is larger than the desired period, and remains constant otherwise.

40. A signal generator according to Claim 36, further comprising a control circuit for verifying the following inequality and producing a first control signal if the inequality is not verified:

$$0 \leq (TC0+TC1) + (TD0(1)+TD1(1)) - (TD0(NL)+TD1(NL))$$

wherein:

TC0+TC1 is a propagation time of a first logic value and a second logic value in a cell within said first group of cells,

TD0(1)+TD1(1) is a propagation time of a first logic value and a second logic value in a least significant cell within said second group of cells, and

TD0(NL)+TD1(NL) is a propagation time of a first logic value and a second logic value in a most significant cell within said second group of cells.

41. A signal generator according to Claim 40, wherein said control circuit comprises:

a reference oscillator for providing a signal with a reference period proportional to (TC0+TC1) + (TD0(1)+TD1(1));

a first measurement oscillator for providing a signal having a measured period proportional to (TD0(NL)+ TD1(NL)); and

a first comparison circuit for comparing the measured period with a reference period and for providing the first control signal if the measured period is smaller than the reference period.

42. A signal generator according to Claim 41, wherein said control circuit further comprises:

a second measurement oscillator for providing a signal having a second measured period proportional to (TD0(NL-1)+TD1(NL-1)); and

a second comparison circuit for comparing the second period with the reference period, and for providing a second control signal if the measured period is less than the reference period.

43. An oscillator for providing an output signal from an N-bit control number, with N being an integer greater than 1, the oscillator comprising:

a first group of cells, each cell comprising at least one inverter;

a first selection circuit connected to said first group of cells for selecting a number of cells as a function of predetermined most significant bits of the control number;

a second group of cells, each cell comprising at least one inverter; and

a second selection circuit connected to said second

group of cells for selecting one of the cells as a function of predetermined least significant bits of the control number;

the selected cells of said first and second groups being connected in series to form a chain of inverters.

44. An oscillator according to Claim 43, wherein each cell within said second group of cells is assigned a place value j ranging from 1 to NL, and wherein said second selection circuit comprises NL switches controlled by signals representing the least significant bits of the control number, each switch for being connected in series between an input and an output of a cell having a same place value j.

45. An oscillator according to Claim 43, wherein two different cells of said second group of cells have different propagation times for a first logic value and a second logic value.

46. An oscillator according to Claim 43, wherein a difference between a propagation time of a first logic value and a second logic value in a cell within said second group of cells with a place value j and that of a cell within said second group of cells with a place value j-1 is less than a desired uncertainty for a period of the output signal.

47. An oscillator according to Claim 43, wherein when the control number increases by 1, a cell within said second group of cells with a place value j is selected, this selected cell being at least one of a cell having a place value immediately higher than that of a previously selected cell within said second group of cells, and a cell with a

lower place value, with an additional cell within said first group of cells also being selected.

48. A method for generating an output signal comprising:

comparing a period of the output signal with a desired period for providing an N-bit control number;

decoding least significant bits of the N-bit control number for providing a first set of control signals;

decoding most significant bits of the N-bit control number for providing a second set of control signals; and

providing the output signal based upon the N-bit control number, with N being an integer greater than 1, using an oscillator comprising a first group of cells, each cell comprising at least one inverter and a first selection circuit connected to the first group of cells, and a second group of cells, each cell comprising at least one inverter and a second selection circuit connected to the second group of cells, the providing comprising

selecting a number of cells within the first group of cells based upon the second set of control signals, and

selecting one of the cells within the second group of cells based upon the first set of control signals,

the selected cells of the first and second groups being connected in series to form a chain of inverters.

49. A method according to Claim 48, wherein each cell within the second group of cells is assigned a place

value j ranging from 1 to NL, and wherein the second selection circuit comprises NL switches controlled by the first set of control signals.

50. A method according to Claim 48, wherein two different cells within the second group of cells have different propagation times for a first logic value and a second logic value.

51. A method according to Claim 48, wherein a difference between a propagation time of a first logic value and a second logic value in a cell within the second group of cells having a place value j and that of a cell within the second group of cells having a place value j-1 is less than a desired uncertainty for a period of the output signal.

52. A method according to Claim 48, wherein when the control number increases by 1, a cell within the second group of cells having a place value j is selected, this selected cell being at least one of a cell having a place value immediately higher than that of a previously selected cell within the second group of cells, and a cell with a lower place value, with an additional cell within the first group of cells also being selected.

53. A method according to Claim 48, wherein the control number increases if the period of the output signal is less than the desired period, decreases if the period of the output signal is larger than the desired period, and remains constant otherwise.

In re Patent Application of:
GAILHARD ET AL.
Serial No. **Not yet assigned**
Filing Date: **Herewith**

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REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

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EXPRESS MAIL NO: EL747059541US

DATE OF DEPOSIT: October 30, 2001

NAME: Regan Sampson

SIGNATURE:

SUBMISSION OF PROPOSED MODIFICATIONS TO DRAWINGS

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Submitted herewith is a request for proposed drawing modifications as indicated in red ink to label the blocks in FIGS. 1-5. FIGS. 1, 3 and 5 are being further amended to better illustrate the plurality of lines between the applicable blocks.

Respectfully submitted,

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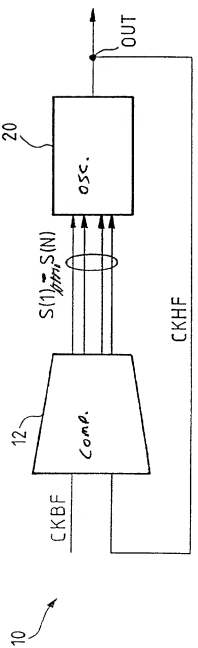


FIG_1
Prior Art

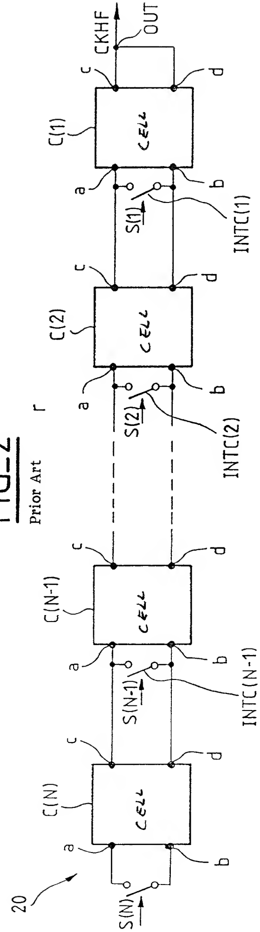
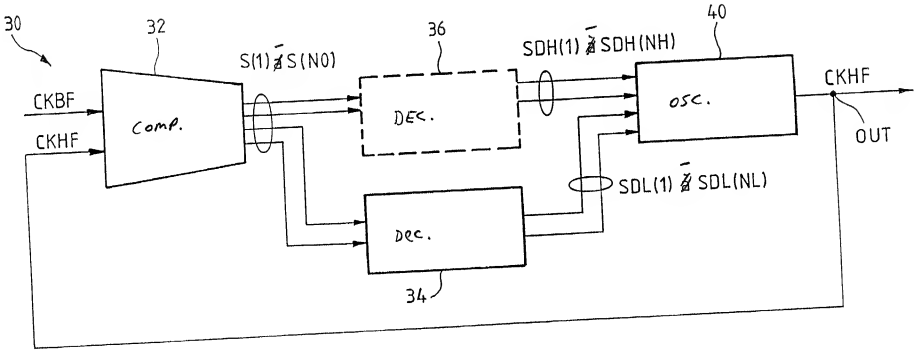


FIG_2
Prior Art

FIG_3



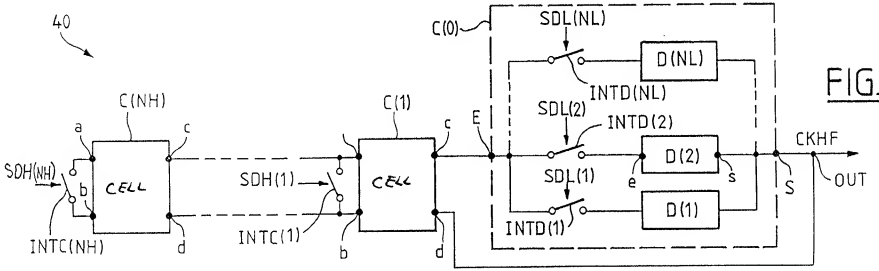
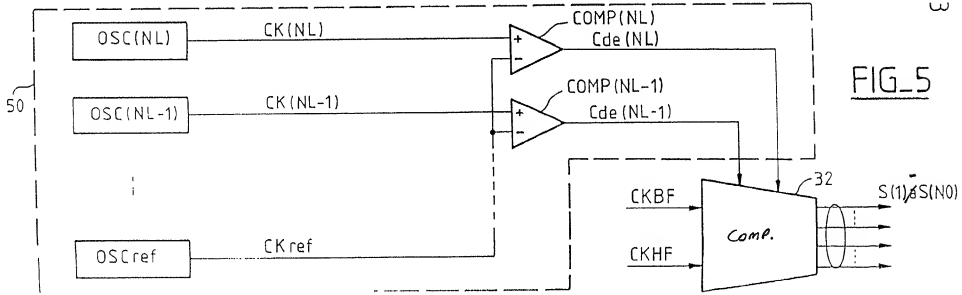

40
C(NH)
C(1)
C(0)
SDL(NL)
D(NL)
INTD(NL)
SDL(2)
INTD(2)
D(2)
SDL(1)
D(1)
INTD(1)
CKHF
OUT
SDH(NH)
CELL
SDH(1)
INTC(NH)
INTC(1)
a
b
c
d
e
s
E
S

FIG_4


50
OSC(NL)
CK(NL)
COMP(NL)
Cde(NL)
OSC(NL-1)
CK(NL-1)
COMP(NL-1)
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OSCref
CKref
CKBF
CKHF
Comp.
32
S(1)
S(N0)

FIG_5

3/3